REMARKS/ARGUMENTS

Claims 1-27 were pending in the present application. Upon entry of this amendment, claims 1, 8, and 24 are amended leaving claims 1-27 pending consideration. Under 35 U.S.C. 103(a) claims 1-9, 13, 18, 20, 21, and 23-27 stand rejected as being obvious in view of U.S. Patent Application Publication No. 2020159483 published to Clauberg (hereinafter "Clauberg") in view of U.S. Patent No. 5,652,878 issued to Craft (hereinafter "Craft"), in further view of U.S. Patent No. 6,919,736 issued to Agrawal et al. (hereinafter "Agrawal"), claims 2, 9, and 13 stand rejected over Clauberg, Craft, and Agrawal in further view of U.S. Patent No. 6,747,886 issued to Morikawa (hereinafter "Morikawa"), and claim 21 stands rejected over Clauberg, Craft, and Agrawal, in further view of U.S. Patent No. 6,160,419 issued to Veenstra (hereinafter "Veenstra"). Claims 10-12, 14-17, 19 and 22 are objected to. A request for continued examination is submitted herewith to allow entry of this amendment.

Applicants aver that no new matter has been added in this response.

Examiner Interview

Applicants appreciate the interview with the Examiner December 6, 2006, where claim amendments, claim objections, and the cited art were discussed in general.

§103 Rejections

Claims 1, 8, and 24

In the Office Action, under 35 U.S.C §103(a) the Examiner rejected claims 1-9, 13, 18, 20, 21, and 23-27 over Clauberg in view of Craft and Agrawal, and rejected claims 2, 9, and 13 over Clauberg, Craft, and Agrawal, in further view of Morikawa, and rejected claim 21 over Clauberg, Craft, and Agrawal, in further view of Veenstra.

With regard to claims 1, 8, and 24 the Examiner states that Clauberg in combination with Craft and Agrawal teaches a method of receiving a serial stream of data bits, deserializing the stream of data bits, inputting the parallel bits into a register via a de-multiplexer, inputting an output of the first register to a second register, providing the parallel

bits in a plurality of parallel bit output formats, where the shift register is capable of shifting the outputted data into any of the plurality of parallel formats, selecting one of the subsets and associated parallel bit outputs based on match flag outputs from the content addressable memory, and the data lines being grouped into a plurality of overlapping subsets of the bus, citing paragraph 23, and paragraph 32, and Figure 2, *et seq.* of Clauberg, columns 2 and 3 *et seq.* of Craft, Figure 3 and column 3 *et seq.* of Morikawa, column 1 and 2, *et seq.* of Veenstra, and column 12, and the abstract *et seq.* of Agrawal. These rejections are respectfully traversed.

Applicants submit that Clauberg, Craft, Agrawal, Morikawa, and Veenstra alone or in combination do not disclose all of the elements of claim 1, 8, or 24. For example, claim 1 as amended recites in part" inputting outputs of [] first and second registers to [a] content addressable memory, wherein [] parallel bits, output of the first register, and output of the second register are combined and stored as a first parallel word in a first row of the content addressable memory; providing a bus configured to receive the parallel bits and output of the first register, wherein the data lines forming the bus are grouped into a plurality of overlapping subsets of the bus that each contain at least one common data line...providing a set of parallel words stored in the content addressable memory, wherein at least one of the set of parallel words includes a fixed frame alignment detection pattern...simultaneously comparing the first parallel word to the set of parallel words stored in the content addressable memory to detect a frame alignment pattern in the first parallel word...when the frame alignment pattern is detected, selecting one of the subsets and associated parallel bit outputs based on match flag outputs from the content addressable memory, wherein each of the match flag outputs are associated with a respective one of the set of parallel words that includes the matching frame alignment pattern, claim 8 recites in part "a content addressable memory, coupled to the shift register to receive [a] first parallel data output in parallel, wherein the parallel output of the shift register is stored as part of a first parallel word in a first row of the content addressable memory that is simultaneously compared to a set of parallel words employed by the content addressable memory to detect a pattern within the first parallel word, wherein each parallel word of the set of parallel words includes a fixed data pattern to detect the pattern in the first parallel word, wherein each fixed data pattern

includes a respective data position within a respective data word", and claim 24 recites in part "generating a third parallel word from [a] combination of [a] first parallel word and [a] second parallel word, wherein the third parallel word is wider than the first parallel word and second parallel word; storing the third parallel word in a first row of a content addressable memory; detecting a frame alignment symbol within the third parallel word by simultaneously comparing the third parallel word to a plurality of fixed frame alignment patterns, wherein each of the frame alignment patterns are part of a respective one of a set of parallel words stored in the content addressable memory."

Clauberg discloses deserializing an incoming serial data stream into a 16 bit parallel data stream using a deserializer. The 16 bit parallel data output stream is converted to an unaligned 64 bit word stored in a first register 214. Over three clock cycles, three 64 bit words are stored in a second register to form a 192 bit word. An align position detection unit 218 locates the specific bit pattern indicating the beginning of a new frame (e.g., A1A2) by "hunting" along the 192 bit word to find the correct 64 bit section. Clauberg does not disclose how the align position detection unit operates. An extraction unit 222, extracts a smaller the 64 bit section of the 192 bit word and sends that to an output port 204.

Craft discloses a data compression engine. In Craft, a CAM and comparator are used to compare incoming data received with previously received data from the incoming data stream that is stored in the CAM, and then store the latest incoming data for future comparisons to incoming data yet to be received to generate a compressed word token. Craft relies on the comparator circuit and a write select shift register to compare data words received with other previously received data words to detect a match and generate a compressed word token. Craft and Clauberg are therefore not properly combinable, as Craft's configuration would defeat Clauberg's attempt to generate an aligned data stream having a predetermined width as the token generated would combine data in a compressed form removing the alignment position characteristic and requiring an additional decompression step not disclosed by Clauberg nor Craft to generate the aligned data stream (see Craft col. 4, lines 34-64).

Morikawa discloses a level sifting circuit. Veenstra discloses a CAM to store keywords associated with datawords stored in another functional block. In Veenstra, if a request dataword matches one of the keywords, the second functional block outputs the dataword stored therein associated with the matching keyword.

Agrawal teaches away from a bus having subsets that share a common data line as each of the subsets are mutually exclusive (i.e., they do not share a common data line), the overlap refers to a mode (i.e., shallow-and-wide mode) where a data bus is used to support a single wide word that does not use subsets (see Agrawal Abstract, col. 12 lines 19-28). Therefore, Agrawal is not properly combinable with the cited references. Even if Agrawal could be combined, in the mode where subsets are used in Agrawal (i.e., the deep-and-narrow mode), they do not share a common data line which would defeat the purpose of having subsets of a bus that share a common data line. Therefore, Applicants submit that Craft, Morikawa, Veenstra, and Agrawal fail to make up for what Clauberg lacks.

Applicants therefore submit that Clauberg, Craft, Agrawal, Morikawa, and Veenstra, alone or in combination, do not disclose *simultaneously comparing a first parallel word to a set of parallel words stored in a content addressable memory having a fixed frame alignment pattern with a data position to detect a frame alignment pattern in the first parallel word, and when the frame alignment pattern is detected, selecting a subset of overlapping subsets of a bus containing a common data line and associated parallel bit outputs based on match flag outputs from the content addressable memory that are associated with which of the set of parallel words contains a matching frame alignment pattern and data position* as claimed (emphases added).

Therefore, as claims 1, 8, and 24 disclose elements not disclosed by Clauberg, Craft, Agrawal, Morikawa, and Veenstra, taken alone or in combination, Applicants submit claims 1, 8, and 24 are allowable over those references.

Dependent Claims 2-7, 9-23, and 25-27

Claims 2-7 depend from amended claim 1, claims 9-23 depend from claim 8, and claims 25-27 depend from claim 24 and are therefore patentable for at least the above reasons discussed with respect to claims 1, 8, and 24 as well as the limitations they recite.

Allowable Subject Matter

In the Office Action, the Examiner objected to the claims. The Examiner stated that claims 10-12, 14-17, 19, and 22 are objected to but would be allowable if written in independent form.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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